

## Refine Search

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L11





### Search History

DATE: Friday, August 06, 2004    [Printable Copy](#)    [Create Case](#)

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<i>DB=USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>			
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<u>L10</u>	L8 same (device or chip or ic)	23	<u>L10</u>
<u>L9</u>	L6 same voltage	80	<u>L9</u>
<u>L8</u>	L6 same current	65	<u>L8</u>
<u>L7</u>	L6 same adjust\$	6	<u>L7</u>
<u>L6</u>	L1 same circuit same measur\$	116	<u>L6</u>
<u>L5</u>	L3 same l1	9	<u>L5</u>
<u>L4</u>	l1 and l1	6429	<u>L4</u>
<u>L3</u>	self-test\$	8991	<u>L3</u>
<u>L2</u>	L1 same measur\$ same \$test\$	24	<u>L2</u>
<u>L1</u>	internal near2 power near2 supply	6429	<u>L1</u>

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L2: Entry 11 of 24

File: USPT

Apr 7, 1998

DOCUMENT-IDENTIFIER: US 5736894 A

TITLE: Semiconductor device and method of adjusting internal power supply potential of the semiconductor device

Detailed Description Text (14):

First, test mode signal .phi.1 is set to the "L" level, test mode signal .phi..sub.2 is set to the "H" level so that  $V_{\text{sub.2}} = 0V$ , and internal power supply potential intVcc is measured at a point where  $\text{extVcc} = V_a$ . At this time, since  $V_{\text{sub.2}} = 0V$ , it holds that  $\text{intVcc} = V_{\text{sub.1}}$ . Thereafter, difference voltage  $\Delta a$  between the set value of  $V_{\text{sub.1}}$  and the measured value of  $\text{intVcc} = V_{\text{sub.1}}$  at the point where  $\text{extVcc} = V_a$  is calculated, and resistance values  $R_{\text{sub.3}}$  and  $R_{\text{sub.1}}$  of variable resistance circuits 8 and 15 are adjusted, whereby  $V_{\text{sub.1}}$  is raised by difference voltage  $\Delta a$ . Consequently, the curve  $V_{\text{sub.N1}}$  of FIG. 2 can be corrected to the line of  $V_{\text{sub.N1}}$ .

Detailed Description Text (15):

Thereafter, test mode signal .phi..sub.1 is set to "H" level, test mode signal .phi..sub.2 is set to the "L" level so that  $V_{\text{sub.1}} = 0V$ , and internal power supply potential intVcc where  $\text{extVcc} = V_b$  is measured. At this time, since  $V_{\text{sub.1}} = 0V$ , it holds that  $\text{intVcc} = V_{\text{sub.2}}$ . Thereafter, difference voltage  $\Delta b$  between the measured value of  $\text{intVcc} = V_{\text{sub.2}}$  and the set value of  $V_{\text{sub.2}}$  at the point where  $\text{extVcc} = V_b$  is calculated, resistance values  $R_{\text{sub.4}}$  and  $R_{\text{sub.2}}$  of variable resistance circuits 19 and 22 are adjusted and thus  $V_{\text{sub.2}}$  is lowered by the difference voltage  $\Delta b$ . Thus the line  $V_{\text{sub.N2}}$  of FIG. 3 can be corrected to the curve  $V_{\text{sub.N2}}$ .

Detailed Description Text (29):

First, in the similar manner as in Embodiment 1, the difference voltage  $\Delta a$  between the set value of  $V_{\text{sub.1}}$  and the measured value at the point where  $\text{extVcc} = V_a$  is calculated. Thereafter, test mode signal .phi..sub.3 is set to the "H" level so that P channel MOS transistor 37 is rendered non-conductive. Consequently, series resistance value of variable resistance circuit 8 and test circuit 26 increases from  $R_{\text{sub.3}}$  to  $R_{\text{sub.3}} + \phi.R_{\text{sub.3}}$ , current value  $I_{\text{sub.1}}$  reduces and  $V_{\text{sub.1}}$  lowers. The characteristic part of internal power supply potential intVcc at this time corresponds to  $V_{\text{sub.N11}}$  of FIG. 5. The internal power supply potential intVcc =  $V_{\text{sub.1}}$  at the point where  $\text{extVcc} = V_a$  is measured, and the difference voltage  $\Delta a_{\text{sub.1}}$  of  $V_{\text{sub.1}}$  before and after the test mode signal .phi..sub.3 is set to "H" level is calculated. More specifically, the change  $\Delta a_{\text{sub.1}}$  of  $V_{\text{sub.1}}$  with respect to the change  $\Delta R_{\text{sub.3}}$  of the resistance value of constant current circuit 32 is actually measured.

Detailed Description Text (30):

Thereafter, test mode signal .phi..sub.3 is recovered to the "L" level, and test mode signal .phi..sub.4 is set to "L" level. Consequently, series resistance value of variable resistance circuit 15 and test circuit 27 increases from  $R_{\text{sub.1}}$  to  $R_{\text{sub.1}} + \Delta R_{\text{sub.1}}$ , and  $V_{\text{sub.1}}$  rises. The characteristic curve of internal power supply potential intVcc at this time corresponds to  $V_{\text{sub.N12}}$  of FIG. 5. At this state, internal power potential  $\text{intVcc} = V_{\text{sub.1}}$  is measured at a point where  $\text{extVcc} = V_a$ , and difference voltage  $\Delta a_{\text{sub.2}}$  before and after the test mode signal .phi..sub.4 is set to the "H" level is calculated. In other words, the

change  $\Delta a_{sub.2}$  of  $V_{sub.1}$  with respect to the change  $\Delta R_{sub.1}$  of the resistance value of  $V_{sub.2}$  generating circuit 33 is actually measured. It is possible to correct the deviation of  $V_{sub.1}$  from the set value, based on the two values  $\Delta a_{sub.1}$  and  $\Delta a_{sub.2}$ . FIG. 5 shows an example in which the measured value is lower than the set value of  $V_{sub.1}$ . In that case, by increasing resistance value  $R_{sub.1}$  of  $V_{sub.1}$  generating circuit 33,  $V_{sub.1}$  can be corrected. The necessary value of correction of the resistance in this case is represented as  $(\Delta a / \Delta a_{sub.2}) \times \Delta R_{sub.1}$ . Conversely, if the measured value of  $V_{sub.1}$  is higher than the set value, resistance value  $R_{sub.3}$  of constant current circuit 32 is increased and current  $I_{sub.1}$  is reduced so that  $V_{sub.1}$  is lowered to be equal to the set value. The necessary value of correction of the resistance in this case is represented as  $(\Delta a / \Delta a_{sub.1}) \times \Delta R_{sub.3}$ .

Detailed Description Text (31):

The method of adjusting  $V_{sub.2}$  will be described. First, in the similar manner as Embodiment 1, difference voltage  $\Delta b$  between the set value and the measured value of  $V_{sub.2}$  at the point where  $ExtV_{cc} = V_a$  is calculated. Thereafter, test mode signal  $\phi_{sub.6}$  is set to the "H" level so that P channel MOS transistor 43 is rendered non-conductive. Consequently, series resistance value of variable resistance circuit 22 and test circuit 29 increases from  $R_{sub.2}$  to  $R_{sub.2} + \Delta R_{sub.2}$ , and  $V_{sub.2}$  lowers from  $extV_{cc} - I_{sub.2} \times R_{sub.2}$  to  $extV_{cc} - (R_{sub.2} + \Delta R_{sub.2})$ . Characteristic curve of the internal power supply potential  $IntV_{cc}$  at this time corresponds to  $V_{sub.N21}$  of FIG. 6. At this state, the internal power supply potential  $intV_{cc} = V_{sub.2}$  at the point where  $extV_{cc} = V_b$  is measured, and difference voltage  $\Delta b_1$  of  $V_{sub.2}$  before and after the test mode signal  $\phi_{sub.6}$  is set to the "H" level is calculated. In other words, the change  $\Delta b_{sub.1}$  of  $V_{sub.2}$  with respect to the change  $\Delta R_{sub.2}$  of the resistance value of  $V_{sub.2}$  generating circuit 35 is actually measured.

Detailed Description Text (32):

Thereafter, test mode signal  $\phi_{sub.6}$  is returned to the "L" level, and test mode signal  $\phi_{sub.5}$  is set to the "H" level. Consequently, series resistance value of variable resistance circuit 19 and test circuit 28 increases from  $R_{sub.4}$  to  $R_{sub.4} + \Delta R_{sub.4}$ , current value of  $I_{sub.2}$  reduces and  $V_{sub.2}$  increases. The characteristic curve of internal power supply potential  $intV_{cc}$  at this time corresponds to  $V_{sub.N22}$ . At this state, internal power supply potential  $intV_{cc} = V_{sub.2}$  at the point where  $extV_{cc} = V_b$  is measured, and difference voltage  $\Delta b_{sub.2}$  before and after the test mode signal  $\phi_{sub.5}$  is set to the "H" level is calculated. In other words, the change  $\Delta b_{sub.2}$  of  $V_{sub.2}$  with respect to the change  $\Delta R_{sub.4}$  of the resistance value of the constant current circuit 34 is actually measured.

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US005736894A

## United States Patent [19]

Suwa

[11] Patent Number: 5,736,894

[45] Date of Patent: Apr. 7, 1998

[54] SEMICONDUCTOR DEVICE AND METHOD OF ADJUSTING INTERNAL POWER SUPPLY POTENTIAL OF THE SEMICONDUCTOR DEVICE

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5,426,616 6/1995 Kajigaya et al. .... 365/226  
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5,554,953 9/1996 Shibayama et al. .... 327/541

[75] Inventor: Makoto Suwa, Hyogo, Japan

## FOREIGN PATENT DOCUMENTS

[73] Assignee: Mitsubishi Denki Kabushiki Kaisha, Tokyo, Japan

4-263193 9/1982 Japan .

[21] Appl. No.: 559,052

Primary Examiner—Timothy P. Callahan

Assistant Examiner—Jung Ho Kim

[22] Filed: Nov. 16, 1995

Attorney, Agent, or Firm—Lowe, Price, LeBlanc & Becker

[30] Foreign Application Priority Data

Apr. 26, 1995 [JP] Japan ..... 7-102254

[51] Int. Cl.<sup>6</sup> ..... G05F 1/10

[52] U.S. Cl. .... 327/538; 327/530; 327/540

[58] Field of Search ..... 327/530, 538, 327/540, 543, 535, 541; 365/189.09

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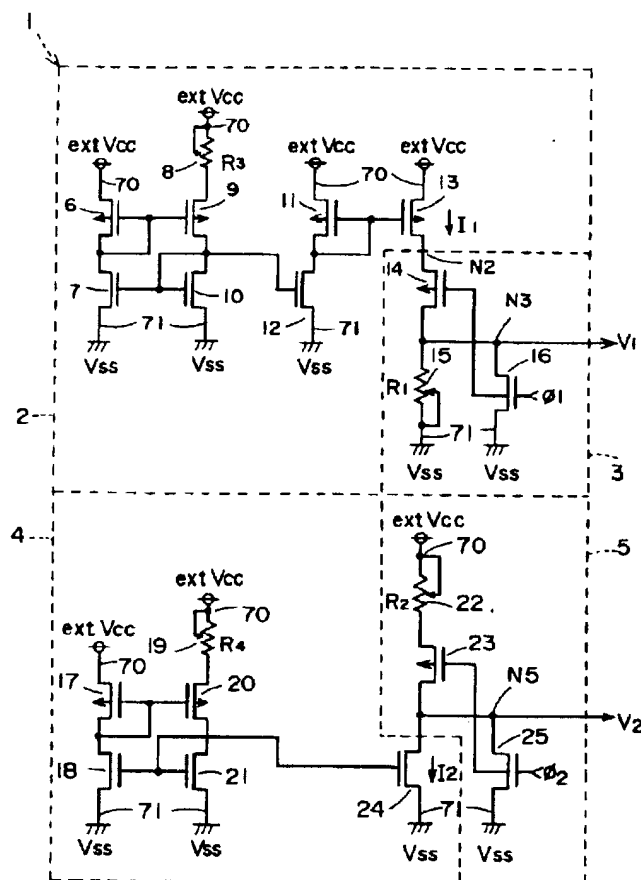
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## [57] ABSTRACT

In a level generating circuit 1 included in an internal power supply circuit of a DRAM, MOS transistors 14 and 16 for inactivating a  $V_1$  generating circuit 3, and MOS transistors 23 and 25 for inactivating a  $V_2$  generating circuit 5 are provided. When  $V_1$  is to be adjusted,  $V_2$  generating circuit 5 is inactivated, and when  $V_2$  is to be adjusted,  $V_1$  generating circuit 3 is inactivated. Therefore, failure of adjustment of internal power supply potential  $\text{intVcc}$  caused by confusion of  $V_1$  and  $V_2$  can be prevented.

10 Claims, 10 Drawing Sheets



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L5: Entry 1 of 9

File: USPT

Mar 11, 2003

DOCUMENT-IDENTIFIER: US 6532183 B2

TITLE: Semiconductor device capable of adjusting internal potential

Detailed Description Text (3):

FIG. 1 is a block diagram showing the structure of a system LSI 1 according to a first embodiment of the present invention. Referring to FIG. 1, this system LSI 1 comprises a logic circuit part 2, a memory circuit part 3, an internal power supply potential generation circuit 4 and a BIST (built-in self-testing) circuit 5.

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